Q1

Translate the following C code segment to MIPS Assembly program *(Ignore runtime exception on overflow)*. Assume A,B, and C are assigned to $s1, $s2, and $s3 respectively. *(Use other registers if needed).*

```
int A,B,C;
.
 if(A<B)
    C=C+0x8A9FC4;
else
    C=C-A;
.
```

Solution:

```
        .
       slt $t0,$s1,$s2
       beq $t0,$zero,else
       lui $t1,0x008a
       ori $t1,$t1,0x9fc4
       addu $s3,$s3,$t1
       j exit
else:   subu $s3,$s3,$s1
exit:   .
```

Q2

What is the content of each register listed in the table below after executing the following MIPS assembly program?. (*Assume that the memory is organized as a big-endian byte order).*

```
lw $s3,-4($t0)

addi $t0,$t0,-2

lb  $s1,1($t0)

srl $s2,$s3,0xB

lbu $s0,5($t0)

sltu $t1,$s0,$s1
```

Register	Contents 32-bit
$t0	~~0×00010100~~ 0X000100FE
$t1	0X00000001
$s0	0X000000CA
$s1	0XFFFFFF81
$s2	0x000449db
$s3	0x224ED981

Address	Data
0×100FC	0x22
0×100FD	0x4E
0×100FE	0xD9
0×100FF	0x81
0×10100	0xC7
0×10101	0x56
0×10102	0x80
0×10103	0xCA

Q3- (4pts)

Consider a Program P1 executes 5×10^9 instructions in 2 sec on a computer M1 with a clock rate 4 GHz, and the same program executes 6×10^9 instructions in 1.5 sec on a computer M2 with a clock rate 6 GHz. Find : -

a. Instruction execution rate (instruction per second) for each computer when running program P1. ***(1pt)***
   P1 executes 5×10^9 instructions in 2 sec on M1--> per sec it executes 2.5×10^9 IPS (instruction per second)
   P1 executes 6×10^9 instructions in 1.5 sec on M2--> per sec it executes 4×10^9 IPS (instruction per second)

b. Average CPI for P1 on both computers. ***(1pt)***
   CPU_ex_time = CPI x IC / CLock rate
   $CPI_{P1\_M1} = 2 \times4\times10^9/(5\times10^9) = 8/5=1.6$ cycles per instruction.
   $CPI_{P1\_M2} = 1.5 \times6\times10^9/(6\times10^9) = 8/5=1.5$ cycles per instruction.

c. Suppose a program P2 runs 5 sec on a computer M1, and it has the same CPI of P1 on each computer M1 and M2. Find the instruction count of P2 for both computers if M1 is two times faster than M2 when executing P2. ***(2pts)***

$CPI_{P2\_M1} = CPI_{P1\_M1} = 1.6$
$CPI_{P2\_M2} = CPI_{P1\_M2} = 1.5$
$CPU\_ex\_time_{P2\_M1}$ = CPI x IC / CLock rate ===> $IC_{P2\_M1} = 5 * 4\times10^9/1.6 = 12.5\times10^9$ instructions.
M1 is two times faster than M2 ---> Ex_time on M2 = 10 sec.
$IC_{P2\_M2} = 10 * 6\times10^9/1.5 = 40\times10^9$ instructions.

Q4-

Suppose we have two implementations of the same ISA for a given program.
Machine A runs on 2×10^9 cycles per second, and has an average CPI of 1.25.
Machine B clock frequency is 4.2 GHz, and has an average CPI of 2.0.
Which machine is faster for this program, and by how much?

a. Machine A faster than B by 1.3125 times.
b. Machine B faster than A by 1.3125 times.
c. Machine A faster than B by 3.36 times.
d. Machine B faster than A by 3.36 times.

Q5-

Consider a compiler C1 produces 1750 MIPS for a given program on computer M, with three different classes of instructions, Class A, Class B, and Class C, which are require 2, 3, and 5 cycles respectively. The instruction count produced by the first compiler is 5 billion Class A instructions, 1 billion Class B instructions, and 1 billion Class C instructions. If this program is executed by another compiler C2 on the same computer, and it produced 2500 MIPS with same cpu execution time in C1. Calculate:

1. Instruction count produced by compiler C2 =
   a. 11 billion instructions.
   b. 10 billion instructions.
   c. 7 billion instructions.
   d. 9 billion instructions.
2. Clock frequency for Computer M.
   a. 4.5 GHz b. 6.43 GHz c. 3.1 GHz d. 2 GHz
3. Average CPI for a program which is tested by compiler C2.
   a. 1.8.
   b. 2.571.
   c. 18.
   d. 1.

Q6

(a) Translate the following C/C++ code segment to MIPS assembly program. Assume that A, B, C, i, and j are 32-bit signed integer, and they are corresponded to registers $s0, $s1, $s2, $s3, and $s4 respectively ***(12 pts).*** How many instructions are executed if `i==j`.***(4 pts)***,`and if i<j`.***(4 pts)***.

C/C++ code : -

```
if(i == j)
C = C + B;
else
if (i < j)
C = C - A;
else
C = 0;
```

Instructions which are executed if `i==j` : **3 instructions**

Instructions which are executed if `i < j` : **4 instructions**

MIPS assembly program : -

```
      beq $s3,$s4,L2
      slt $t7,$s3,$s4
      bne $t7,$0,L1
      and $s2,$s2,$0
      j exit
L2:   add $s2,$s2,$s1
      j exit
L1:   sub $s2,$s2,$s0
exit: .........
      .........
```

(b) Consider the following MIPS program which is executed and assembled to machine code. Write down the values of the immediate field in binary.***(12 pts)***.

		MACHINE CODE																		
PC	Instruction	OP	Rs	Rt	Immediate field 16-bit															
0x40A8	L1:lui $t0,0x1	001111	00000	01000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x40AC	addi $t0,$t0,-0x7CFF	001000	01000	01000	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1
0x40B0	ori $t0,$t0,0x8301	001101	01000	01000	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1
0x40B4	beq $t0,$0,L1	000100	01000	00000	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0

After execution: `$t0 =` 0x00008301 ***(3 pts).***

Q7

(a) How many gate delays in the carry path of the following 32-bits full adders ***(3pts)***. Which one is the fastest.***(3pts)***

(i) Ripple. — 2 x 32 = 64 gate delay

(ii) Group CLA (8 × 4-bits CLA). — 5 gate delay

(iii) Ripple CLA (8 × 4-bits CLA). — 3 x 8 = 24 gate delay

The fastest 32-bits Full Adder : -

ii. Group CLA